Discover What's Possible™

Anritsu

MX368041B W-CDMA Software
MX368141A HSDPA IQproducer™

(For MG3681A Digital Modulation Signal Generator)

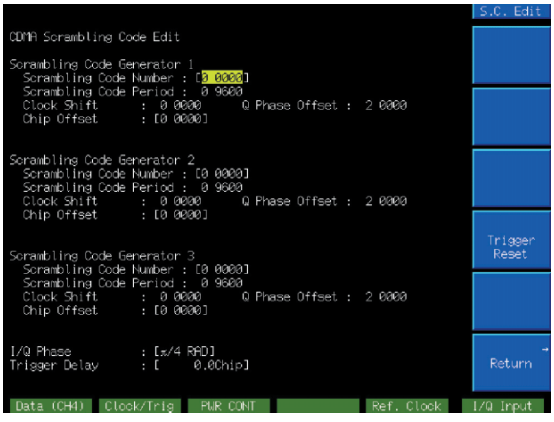
For Evaluating 3GPP (FDD) W-CDMA and HSDPA System

MX368041B W-CDMA Software
3GPP Standard W-CDMA Modulation Signals Outputs

The MX368041B W-CDMA Software is installed in the MU368040A CDMA Modulation Unit, when the MU368040A is housed in the MG3681A Digital Modulation Signal Generator. It can output uplink and downlink of W-CDMA modulation signals for 3GPP (FDD) standard.

Connection with User Equipment and Base Station

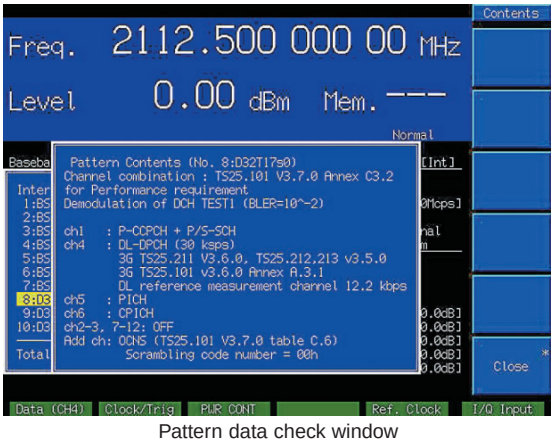
This function can generate P-CCPCH, P-SCH, S-SCH, and CPICH for synchronizing the user equipment (UE) simultaneously to the equivalent of three base stations.
In addition, an external trigger function for controlling the CDMA modulation signal timing is useful in the base station test.



Scrambling code editing

Supports 3GPP Test Specifications

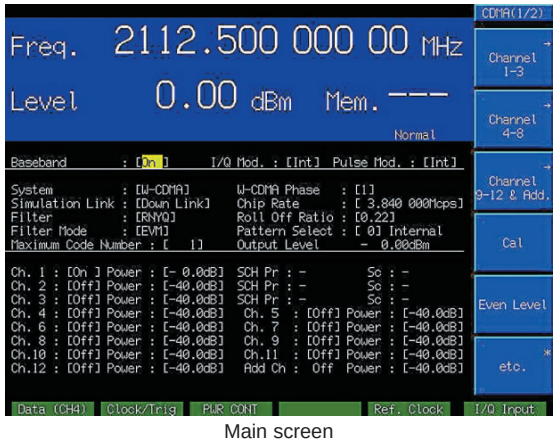
Pattern data based on the 3GPP test specifications, such as base station test models standardized in TS25.141 and downlink multiplex signals with OCNS for maximum input level test standardized in TS25.101, are included in the software. These pattern data can perform modulation based on the test specifications.



Pattern data check window

Multiplex Signals Generation

The signal up to 12 channels can be multiplexed for any settable channel such as the channelization code and code power, etc. And multiplex signals can be added up to 512 channels (at Phase 1).



Main screen

Modulation Data Download Function

The special test pattern and specification updates are supported by the pattern data downloaded from PC memory card. Furthermore, HSDPA signal pattern (Option) supports abundant test patterns for base station test models, multi-carrier, RX test and performance test.

Power Control Function

An external control signal can control the channel power in 1-slot steps. In addition, the code power on each channel can be programmed up to a 64-slot cycle. This is useful for checking the power control operation.

Supports Chip Rates up to 16.5 Mcps

The CDMA modulation signal in the 3GPP specifications can be set chip rates of 1.6 to 16.5 Mcps in 1 cps steps.

Variable Baseband Filter Function

In addition to setting the baseband filter to Nyquist or Root Nyquist, the roll-off ratio can be set from 0.10 to 1.00 in 0.01 steps.

MX368041B W-CDMA Software
Real Time Generation of Modulation Signals in Each Format

Five physical channels and two transport channels can be selected on the screen.
And the each parameter for these channels can be edited and modulation signals can be generated based on various test specifications.

User Equipment Simulation

The DPCCH and DPDCH physical channel formats can be selected. In addition to being able to edit the TFCI and slot format for DPCCH, the TPC bit can be edited in a 60-slot cycle.

DPCCH editing

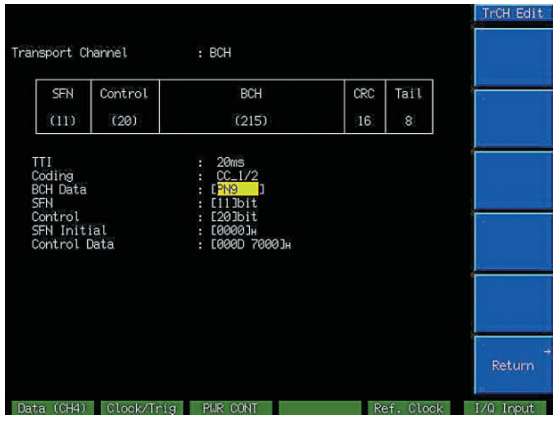
Base Station Simulation

The P-CCPCH, CPICH, DL-DPCH physical channel format can be selected. It is possible to set the open loop Tx diversity (TSTD, STTD) on or off in each channel. In addition to being able to edit the TFCI and slot format for DPCH, the TPC bit can be edited in a 60-slot cycle.

DL-DPCH editing

BCH Editing Function

BCH can be selected in the P-CCPCH data at downlink and be edited. The BCH editing screen is used to edit the SFN bit count, SFN initial, control bit count, etc.



BCH editing

DCH Editing Function

DCH can be selected in the DL-DPCH data at downlink and the DPDCH data at uplink and be edited. The DCH editing screen is used to edit the transport channel count, rate matching attribute, etc. This supports reference measurement channel 12.2/64/144/384 kbps and BTFD specified by 3GPP TS25. 101/104, AMR and ISDN specified by 3GPP TR25.944 etc. It is also possible to insert BER and BLER up to 10% in 0.1% steps.

DCH editing

MX368141A HSDPA IQproducer™ Editing and Creating Signal Patterns

MX368141A HSDPA IQproducer™ is the PC application software that generates 3GPP HSDPA compliant signal patterns outputted from MG3681A Digital Modulation Signal Generator. MG3681A Digital Modulation Signal Generator that has MU368040A CDMA MODULATION UNIT and MX368041B W-CDMA Software is required for the use of generated signal patterns.
With the MX368141A HSDPA IQproducer™, users can generate signal patterns by editing a setting file (csv format) that determines HSDPA-system signal patterns with Excel program and converting the edited setting file.
The generated signal patterns are downloaded into MG3681A Digital Modulation Signal Generator and selected for use.

Easy to generate signal patterns with the setting file included

With the setting file of standard signal patterns (Fixed Reference Channel*) included in the software, users can generate signal patterns easily only by editing the parameter they wish to change.

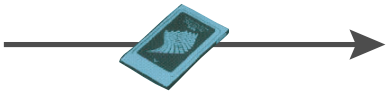
*: Fixed Reference Channel: Down-link standard channel for test of HSDPA indicated by 3GPP TS25.101 Release5.

Easy to switch over signal patterns

Since multiple pattern files that are generated can be downloaded into MG3681A mainframe, users can switch over signal patterns easily by selecting them.

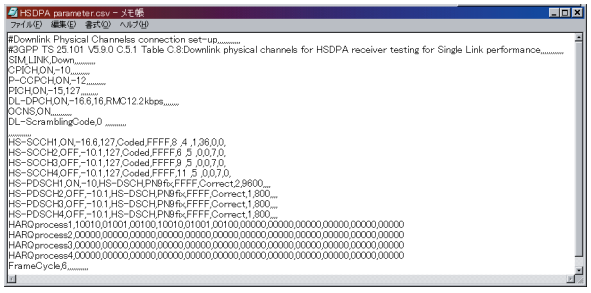
Save the pattern file that is generated by MX368141A HSDPA IQproducer™ and installed in a PC to a memory card and download to MG3681A Digital Modulation Signal Generator.

PC
MX368141A
HSDPA IQproducer™

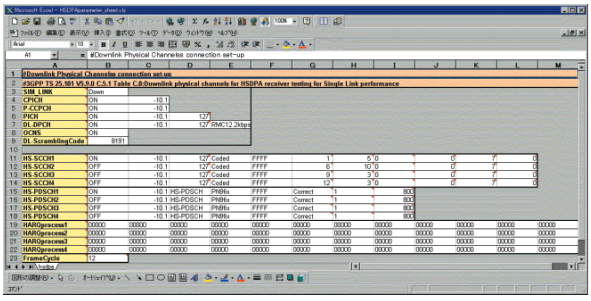


Memory card

MG3681A Digital Modulation Signal Generator
+
MU368040A CDMA Modulation Unit
+
MX368041B W-CDMA Software

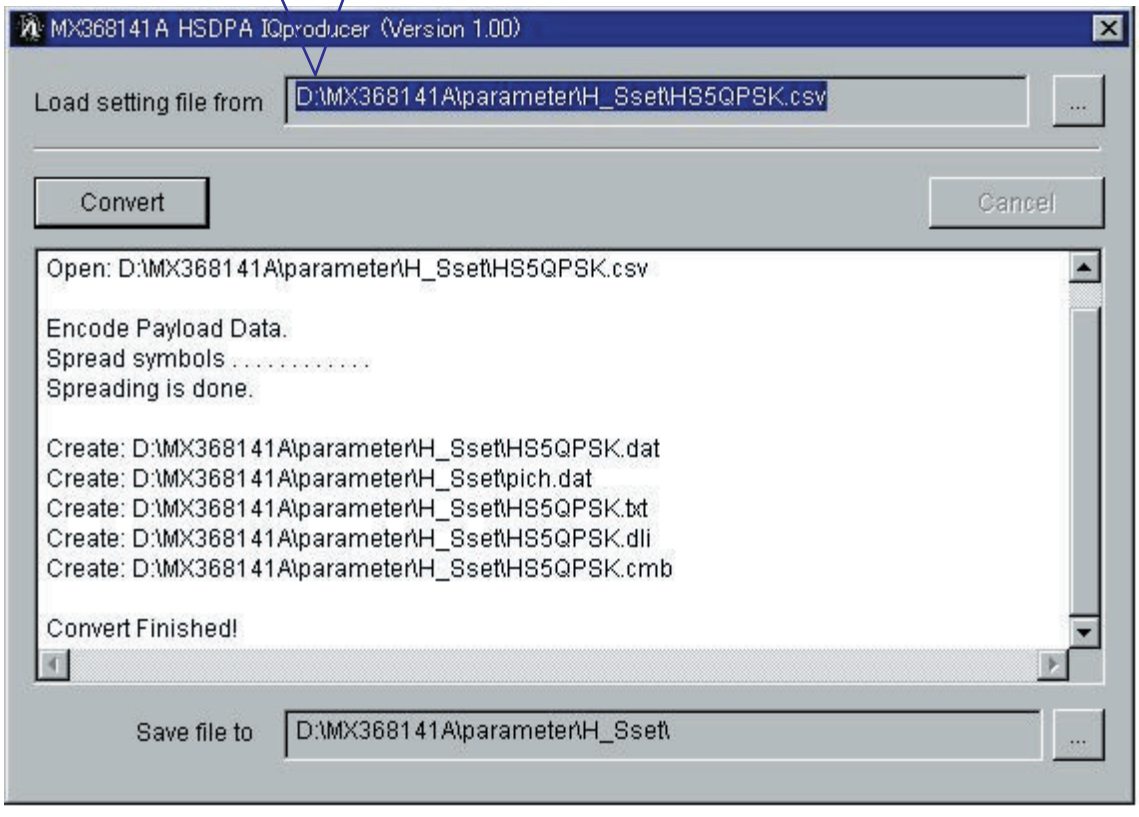


Setting screen in the Plain Text format



Setting screen in the Excel format

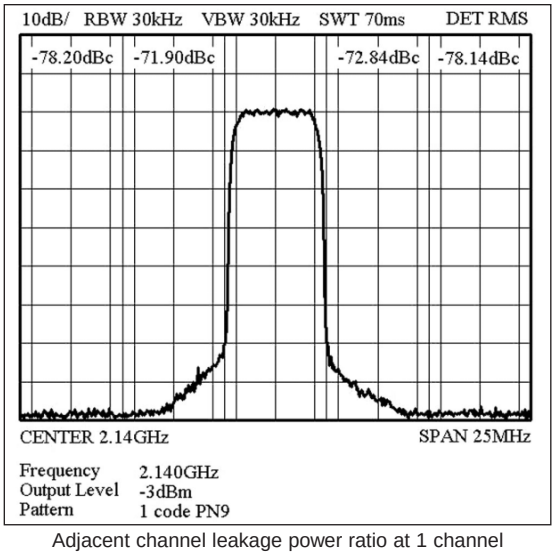
MX368141A HSDPA IQproducer™ setting file edit screen



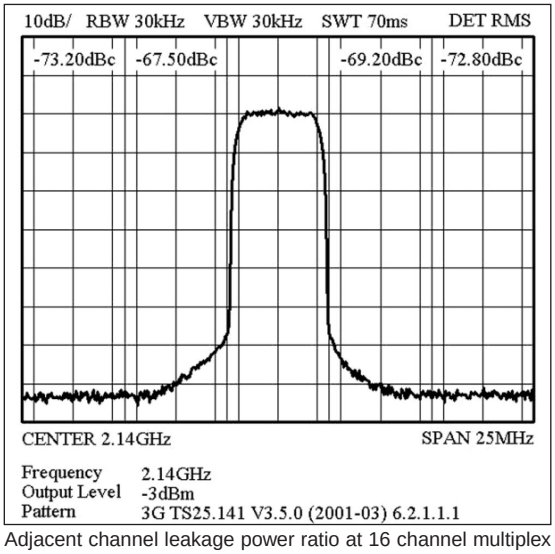
Excellent Analog Performance/Various Options

Adjacent Channel Leakage Power Ratio

The adjacent channel leakage power ratio of the digital modulation signal generator is an important factor in distortion testing of device and interference testing of receivers.
The MG3681A achieves an excellent adjacent channel leakage power ratio by an optimized circuit design. The typical adjacent channel leakage power ratio for W-CDMA system is –68 dBc/3.84 MHz and the secondary adjacent channel leakage power ratio is –75 dBc/3.84 MHz.



Adjacent channel leakage power ratio at 1 channel



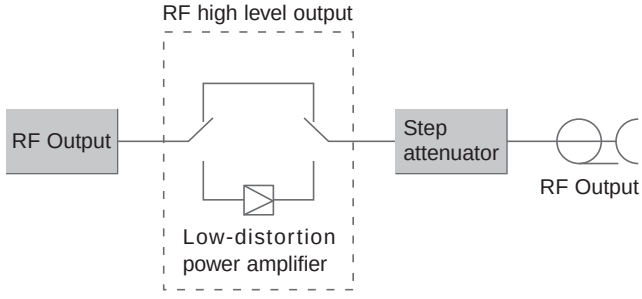
Adjacent channel leakage power ratio at 16 channel multiplex

AWGN Supports Dynamic Range Test

When performing the receiver dynamic range test specified by 3GPP, AWGN with the W-CDMA modulation signal is required. When the MU368060A AWGN Unit is installed in the MG3681A, a high-precision AWGN can be output in the 4 to 16 MHz bandwidth. Moreover, since one MG3681A can output a signal that is the internally added W-CDMA uplink modulation signal and the AWGN, is useful for simple test of the base station receiver dynamic range.

RF Level-up at Modulation

When the RF high level output (Option 42) is installed in the MG3681A, the RF level can be output 8 dB gain without degrading the adjacent channel leakage power ratio in the W-CDMA system frequency band (1.9 to 2.3 GHz). This is very useful for signal source of power amplifier requiring a high input level.



RF high level output option installation diagram

Eliminate to Out-Band Spurious

When outputting a W-CDMA signal at the MG3681A, measurement may sometimes be interfered with by spurious* that is generated due to the circuit composition. In such a case, unwanted signals can be eliminated by connecting the MA2512A Band Pass Filter to the RF output of the MG3681A.
The MA2512A has excellent amplitude and group delay characteristics in the W-CDMA system frequency band (1.92 to 2.17 GHz), so it does not degrade the MG3681A modulation accuracy.

*: 660 MHz, output frequency + 660 MHz, 2nd/3rd harmonics

MA2512A Band Pass Filter

Specifications

• MX368041B W-CDMA Software

This software is installed in the MU368040A.

Supported systems		3GPP (FDD)
Spreading method		Direct spread
Modulation method		Uplink: BPSK (data), HPSK (spreading) Downlink: QPSK (data), QPSK (spreading)
Supported phase		Phase 1, 2, 3 (Phase 2 and 3 only support chip rate)
Number of multiplex channel		Phase 1: 1 to 512, Phase 2: 1 to 1024, Phase 3: 1 to 2048
Spreading factor		Phase 1: 1 to 512, Phase 2: 1 to 1024, Phase 3: 1 to 2048
Chip rate		Phase 1: 1.6 to 4.125 Mcps, Phase 2: 3.2 to 8.25 Mcps, Phase 3: 6.4 to 16.5 Mcps
Symbol rate		Chip rate/Spreading factor
Transfer rate accuracy		MG3681A series main frame reference signal accuracy; external reference signal accuracy at external sync
Filter mode		ACP (adjacent channel leakage power priority), EVM (vector accuracy priority)
Baseband filter		Nyquist/Root Nyquist, roll-off ratio: 0.1 to 1.0 (0.01 steps)
Number of arbitrary setting code		1 to 12 (post-spread processing setting)
Download data		Number of symbol data channel: Max. 2 channels (number of channel able to download physical layer data at coding from outside; max. 9 codes at multi code) Symbol data length: 4M symbols/channel (no power sequence), 1M symbols/channel (with power sequence) Waveform data length Any waveform data: 512 Kwords x 2 channels (1 word = 16 bits)
Internally generate channel format	Base station simulation	P-CCPCH (& SCH) Data: PN9, PN15, PN9 fix, 16 bit repeat, BCH TSTD: On/off STTD: 1, 2 [Data = at BCH selection] SFN: Select as 0 to 16 bits (settable initial value) Control: Select as 0 to 32 bits (input 32 bit data) Data: PN9, PN15, PN9 fix, 16 bit repeat CPICH Antenna: 1, 2 DL-DPCH Slot format: Depends on set spreading factor Data: PN9, PN15, PN9 fix, 16 bit repeat, DCH TPC: 4 frame cyclic pattern TFCI: 0 to 3FFh Antenna: 1, 2 DPCCH/DPDCH power ratio BER: 0% to 10% (0.1% resolution) [Data = at DCH selection] Transport channels: 1 to 8 DTX: fix, flexible Data: PN9, PN15, PN9 fix, 16 bit repeat TTI: 10, 20, 40 ms TrBk Size: Depends on encoder and Tr channel count CRC: 0, 8, 12, 16, 24 bits Coder: No coding, convolution (coding rate: 1/2, 1/3), turbo (coding rate: 1/3) Rate matching attribute: 100 to 300 BER: 0% to 10% (0.1% resolution) BLER: 0% to 10% (0.1% resolution)

MX368041B W-CDMA Software

Internally generate channel format	User equipment simulation	DPCCH Slot format: Depends on spreading factor setting TPC: 4 frame cyclic pattern TFCI: 0 to 3FFh FBI: 4 frame or 2 frame cyclic pattern DPDCH Slot format: Depends on spreading factor setting Data: PN9, PN15, PN9 fix, 16 bit repeat, DCH TPC: 4-frame cyclic pattern TFCI: 0 to 3FFh [Data = at DCH selection] Transport channel: 1 to 8 Data: PN9, PN15, PN9 fix, 16 bit repeat TTI: 10, 20, 40 ms TrBk Size: Depends on encoder and Tr channel count CRC: 0, 8, 12, 16, 24 bit Coder: No coding, convolution (coding rate: 1/2, 1/3), turbo (Coding rate: 1/3) Rate matching attribute: 100 to 300 BER: 0% to 10% (0.1% resolution) BLER: 0% to 10% (0.1% resolution)
Spreading signal	Base station simulation	Channelization code: Any setting for each code Encoding: OVSF Setting range (channelization code No.): 0 to (spreading factor –1) Scrambling code*1 Code: M sequence gold Scrambling code No. setting: 00000h to 3FFFFh
	User equipment simulation	Channelization code: Any setting for each code Encoding: OVSF Setting range (channelization code No.): 0 to (spreading factor –1) Scrambling code*1 Encoding: M sequence gold Scrambling code No. setting: 000000h to FFFFFFh
Internally generated data (without coding)		Pseudo-random pattern (PN9, 15, 23) or any 16 bit repeat (CH11, 12 are max. 32 bit variable cyclic pattern)
Code power setting		–40 to 0 dB, off, 0.1 dB resolution
Power control		Internal program function: Slot power of each channel programmable in 2 to 64 slot cycle (1 dB resolution) External control function: Any code power controllable at external signal (TTL level) synchronized with slot (1 dB resolution)
Offset		Settable frame offset for scrambling code (1 symbol resolution) Settable offset between each scrambling code (1 chip resolution)
IQ phase		IQ output symbol point selection: 0, $\pi/4$ rad
External signal	Input signal	Data: Physical layer (before spread processing) serial data input Frame clock/trigger: External frame sync signal input (adjustable trigger delay) Power control: External power control signal input (any 1 code 1 dB step power control) Reference clock: Chip rate 2^n time baseband sync signal input (n: Phase 1 = 0 to 2, Phase 2 = 0 to 1, Phase 3 = 0) Input connector: TTL Level, BNC connector (front panel)
	Output signal	Data clock: Data sync clock output Data: Symbol data output before diffusion Symbol clock: Symbol clock output synchronized to data Reference clock: Chip rate 2^n times clock output (n: Phase 1 = 0 to 3, Phase 2 = 0 to 2, Phase 3 = 0 to 1) Frame clock: Wireless frame cycle pulse output Slot clock: Time slot cycle pulse output Code: Channelization code and scrambling code exclusive OR Output connector: TTL level, BNC connector (rear panel)
IQ signal	Output level	$\sqrt{I^2 + Q^2}$ = 0.200 V (rms) *Number of max. multiplex: 1, filter mode: EVM, 50 Ω termination, BNC connector (front panel)
	Vector accuracy	≤3% (rms) *Chip rate: 3.84 Mcps, number of max. multiplex: 1, filter mode: EVM, 18˚ to 35˚C

MX368041B W-CDMA Software

RF signal	Frequency range	10 to 3000 MHz
	Output level range	–143 to +5 dBm (number of max. multiplex: 1 to 7), –143 to +13 dBm (Option 42: RF high level output On, 1.9 to 2.3 GHz) –143 to +4 dBm (number of max. multiplex: 8 to 12), –143 to +12 dBm (Option 42: RF high level output On, 1.9 to 2.3 GHz) –143 to +3 dBm (number of max. multiplex: 13 to 15), –143 to +11 dBm (Option 42: RF high level output On, 1.9 to 2.3 GHz) –143 to +2.15 dBm (number of max. multiplex: 16 to 19), –143 to +10.15 dBm (Option 42: RF high level output On, 1.9 to 2.3 GHz) –143 to +2 dBm (number of max. multiplex: 20 to 31), –143 to +10 dBm (Option 42: RF high level output On, 1.9 to 2.3 GHz) –143 to +1 dBm (number of max. multiplex: 32 to 50), –143 to +9 dBm (Option 42: RF high level output On, 1.9 to 2.3 GHz) –143 to 0 dBm (number of max. multiplex: ≥51), –143 to +8 dBm (Option 42: RF high level output On, 1.9 to 2.3 GHz)
	Continuous mode variable range	–10 to +8 dB (number of max. multiplex: 16 to 19 others) –10 to +7.14 dB (number of max. multiplex: 16 to 19)
	Burst on/off ratio	>60 dB ∗1.9 to 2.3 GHz
	Vector accuracy	≤2% (rms) ∗1.9 to 2.3 GHz, 0 dBm, chip rate: 3.84 Mcps, number of max. multiplex: 1, filter mode: EVM, Option 42: RF high level output Off
	Carrier leak	≤–30 dBc ∗1.9 to 2.3 GHz, ≤0 dBm, Option 42: RF high level output Off, 18° to 35°C
	Image rejection	≤–40 dBc ∗1.9 to 2.3 GHz, ≤0 dBm, after calibration, Option 42:RF high level output Off
	Level accuracy	±1.2 dB (compared with CW level) ∗1.9 to 2.3 GHz, chip rate: 3.84 Mcps, number of max. multiplex: 1, scrambling code: On, power control function: Off, Option 42: RF high level output Off
	Adjacent channel leakage power ratio	–64 dBc/3.84 MHz (5MHz offset), –71 dBc/3.84 MHz (10MHz offset) –68 dBc/3.84 MHz (typ. 5MHz offset), –75 dBc/3.84 MHz (typ. 10MHz offset) ∗1.9 to 2.3 GHz, –3 dBm, number of max. multiplex: 1, filter mode: ACP, ACP, 18° to 35°C, spectrum analyzer: RMS detection, (At Option 42: RF high level output On, +5 dBm, typical only)
	Spurious	<–60 dBc ∗1.9 to 2.3 GHz, chip rate: 3.84 Mcps, number of max. multiplex: 1, filter mode: ACP, Option 42: RF high level output Off
Firmware backup space		CDMA: 300 KB, DSP: 250 KB, FPGA: 100 KB

∗1: With 3 generators, select each channel and settable to off. Each generator start timing can be set with a resolution of 1 chip.

• MX368141A HSDPA IQproducer™

System		3GPP HSDPA
Required composition		Mainframe: MG3681A Digital Modulation Signal Generator Extended unit: MU368040A CDMA Modulation Unit Software: MX368040B W-CDMA Software
Operating environment		OS: Windows 2000/XP CPU: Pentium 300MHz or faster Memory size: ≥128MB HDD: Occupation ≤200MB Display: 800 x 600 pixels or more Peripheral equipment: It be possible to read CD-R. It be possible to save in Compact-Flash (PC card adapter is required for download to MG3681A)
Setting parameter, Down-link	CPICH	Channel: ON/OFF Channel Power: –40.0 [dB] to 0.0 [dB] Channelization Code: 0
	P-CCPCH	Channel: ON/OFF Channel Power: –40.0 [dB] to 0.0 [dB] Channelization Code: 1
	P-SCH, S-SCH	Channel: ON/OFF (Dependent on a setup of P-CCPCH) Channel Power of P-SCH: "P-CCPCH setting power"– 3.0 dB Channel Power of S-SCH: "P-CCPCH setting power"– 3.0 dB
	PICH	Channel: ON/OFF Channel Power: –40.0 [dB] to 0.0 [dB] Channelization Code: 0 to 255
	DL-DPCH	Channel: ON/OFF Channel Power: –40.0 [dB] to 0.0 [dB] Channelization Code[*1]: 0 to SF-1 SF (Spreading Factor) varies depending on the setting of DCH format as below. RMC 12.2 kbps = 128 RMC 64 kbps = 32 RMC 144 kbps = 16 RMC 384 kbps = 8 AMR1/AMR2/AMR3 = 128 ISDN = 32 DCH format[*1]: RMC 12.2 kbps/RMC 64 kbps/RMC 144 kbps/RMC 384 kbps/AMR1/AMR2/AMR3/ISDN
	OCNS	Channel: ON/OFF Power: The value that brings the total power to 0 dB when it is combined with all other channels whose channel setting is ON. Composed of 6-code DPCH. Refer to 3GPP TS25.101 C.5.2 OCNS Definition for detail. In OCNS = OFF, total power is set to 0dB, maintaining the ratio of the setting level of each channel.
	Scrambling Code	0 to 8,191

MX368141A HSDPA IQproducer™

Setting parameter, Down-link	HS-SCCH	Number of channels: 4 Channel: ON/OFF Channel Power: –40.0 [dB] to 0.0 [dB] Channelization Code: 0 to 127 Data Type: PN9fix*2/ PN15fix*2/16bitRepeat/Coded 16bitRepeat Data: 0000 to FFFF (hex) Code Offset: 1 to 15 Multi-code Number: 1 to 15 Modulation: 0 (QPSK) or 1 (16QAM) Transport-block Size Information: 0 to 63 Redundancy and constellation version: 0 to 7 UE identity: 0 to 65,535
	HS-PDSCH	Number of channels: 4 Channel: ON/OFF Channel Power: –40.0 [dB] to 0.0 [dB] Data Type: PN9fix*2/PN15fix*2/16bitRepeat/HS-DSCH HS-DSCH Information data: PN9fix/PN15fix/16bitRepeat 16bitRepeat Data: 0000 to FFFF (hex) CRC Error insertion: Correct/Fail Number of HARQ Processes: 1 to 8 Virtual IR Buffer Size: 800 to 304,000
	HARQ process	Number of process cycle: 1 to 12 frame Transmission and DTX edit per sub-frame.
Setting parameter, Up-link	DPCCH	Channel: ON/OFF Channel Power (βc): 1 to 15 Channelization Code: 0 (Phase Q)
	DPDCH	Channel: ON/OFF Channel Power (βd): 1 to 15 Channelization Code: SF/4 (Phase I) Spreading Factor changes according to a setup of DCH_format. RMC = 12.2 kbps: SF = 64 RMC = 64 kbps: SF = 16 RMC = 144 kbps: SF = 8 RMC = 384 kbps: SF = 4 AMR1/AMR2/AMR3: SF = 64 ISDN: SF = 16 DCH format*3: RMC 12.2 kbps/RMC 64 kbps/RMC 144 kbps/RMC 384 kbps/AMR1/AMR2/AMR3/ISDN
	HS-DPCCH	Channel: ON/OFF ACK Power: Δ_{ACK} = 0 to 8 NACK Power: Δ_{NACK} = 0 to 8 CQI Power: Δ_{CQI} = 0 to 8 Channelization Code: 64 (Phase Q) Number of process cycle: 1 to 12 frame HARQ-ACK transmission pattern (ACK, NACK/DTX) and CQI transmission pattern (0 to 30 and DTX) can be edited per sub-frame. The timing offset of HS-DPCCH and DPCCH can be specified.
	Scrambling Code	0 to 16,777,215

∗1: RMCxxxkbps: Be based on 3GPP TS25.101 Release5 A.3 DL Reference Measurement Channel.
AMR1/AMR2/AMR3: Be based on TFCS = #1/2/3 of 3GPP TS25.944 4.1.1.3.1.2 Example for 12.2 kbps data.
ISDN: Be based on 3GPP TS25.944 4.1.1.3.1.6 Example for 64 kbps data

∗2: PN9fix and PN15fix are PN9/PN15 data reset for every sub frame.

∗3: RMCxxxkbps: Be based on 3GPP TS25.104 Release5 A.2 UL Reference Measurement Channel.
AMR1/AMR2/AMR3: Be based on TFCS = #1/2/3 of 3GPP TS25.944 4.1.2.2.1.2 Example for 12.2 kbps data.
ISDN: Be based on 3GPP TS25.544 4.1.2.2.1.6 Example for 64 kbps data.

Ordering Information

Please specify the model/order number, name, and quantity when ordering.

Model/Order No.	Name
	Main frame
MG3681A*1	Digital Modulation Signal Generator (250 kHz to 3000 MHz)
	Option
MG3681A-42	RF high level output (1.9 to 2.3 GHz, 8 dB gain)
	Expansion Units
MU368040A*1	CDMA Modulation Unit
MU368060A*1	AWGN Modulation Unit
	Application Software
MX368041B*2	W-CDMA Software
	Standard accessory
W2089AE	MX368041B operation manual: 1 copy
	Option
MX368041B-11*1	HSDPA Signal Pattern
	Application Software
MX368141A	HSDPA IQproducer*3
	Standard accessory
W2416AE	MX368141A operation manual (booklet): 1 copy
	Application part
MA2512A*1	Band Pass Filter (1920 to 2170 MHz)

*1: Refer to the separate catalogs for the MG3681A, MU368040A, MU368060A, MX368041B-11, and MA2512A.
*2: With Compact Flash™ card (with adapter)
*3: Supplied with CD-ROM (The operation manual is recorded on the electronic file)

Compact Flash™ is a registered trademark of SanDisk Corporation.

Anritsu

Specifications are subject to change without notice.

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